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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/028,276	02/24/1998	SHIGERU ATSUMI	1701.73982	4461

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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/028,276	ATSUMI, SHIGERU	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *10-12 and 15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,21-26,28-30 and 32-41* is/are rejected.

7)☒ Claim(s) *14,27,31 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution

1. Prosecution is hereby reopened based on specific knowledge of a particular reference that indicates the non-patentability of appealed claims. See 37 C.F.R. §1.198 and MPEP §§1214.04, 1214.07 and 1002.02(c).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show transistors having different gate oxide thickness as described in the specification. Specifically, though figures 16A and B do use different reference numerals (14 and 15) to differentiate between the dielectrics, layers 14 and 15 are shown having the same thickness and the same cross-hatching. There is nothing to indicate that 15 is thicker than 14. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: on page 15, line 1, delete "circuits" and insert --terminals-- in its place. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 21-26, 28 and 32-39 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 3-196677 to Soeda. Regarding claim 1, Soeda teaches in figure 1 a semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed (in figure 1, transistors 5', 6', 12' and 13' have thick gate oxide while transistors 14 and 15 have thin gate oxide, see also the translation of the reference, page 3 – Means for Solving Problems – which teaches a device having transistors with thick oxide and transistors with thin oxide formed on a substrate); and

an input/output terminal 8 formed on the semiconductor substrate (see again Means for Solving Problems which indicates the pad is on the substrate), wherein a transistor 12' or 13' physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film (e.g 12'/13' have thick gate oxide while 14 and 15 have the thinnest gate oxide).

Regarding claims 2 and 3, Soeda also teaches in figure 1 a power supply terminal V to which an external power supply voltage is applied and a ground terminal G, wherein a transistor 5' connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film (e.g. 14 and 15) and the transistor 5' has a current path connected between the power supply and ground. Regarding claims 4-7, Soeda teaches that the device also includes an interface circuit 10 comprising transistor 12' which is a transistor other than a transistor with the thinnest gate insulation film, that transistor 12' is connected directly to a power supply terminal and has a current path connected between the power supply and a ground terminal, and is part of an input buffer circuit. Regarding claims 4-6 and 8, Soeda also teach an embodiment in figure 2 where transistor 22, which has a thick gate oxide, is connected directly to an input/output terminal 21, is connected between a power supply terminal V and ground G, and is in an interface circuit 19 which is considered an output buffer (see the translation, page 4, third full paragraph).

Regarding claim 21, Soeda teaches in figure 2 an integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed (transistors 22 and 23 have thick films and transistors 24-27 have thin films); and

an input/output terminal 21 formed on the semiconductor substrate, wherein a transistor (e.g. 22) connected directly to the terminal 21, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film.

Regarding claims 22-26 and 28, Soeda teach in figure 2 that the device further comprises a power supply terminal V, a ground terminal G, such that transistor 22 is connected directly to the power supply terminal and has a current path to ground, that transistor 22 is part of an interface circuit 19, and that the interface circuit is an output buffer circuit.

Regarding claims 32-39, as discussed above, Soeda teaches these limitations including the limitation that the transistor connected directly to the input/output terminal and having a thick gate oxide is always so connected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9, 13, 29, 30, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soeda in view of applicant's admitted prior art as shown in figure 3. Soeda taught the device of claims 4, 24 and 35 as discussed above, including that the interface circuit included transistors having thicker gate oxide than transistors of the internal and protected circuits, but did not expressly teach the device wherein the interface circuit comprised a level shifter and output buffer or that the device comprised a regulator circuit providing a signal to the level shifter.

Applicant's admitted prior art teaches in figure 3, an interface having an output buffer circuit 102 and a level shifter 103 and a regulator circuit 101 which provides a signal to the level shifter, the level shifter converting the signal to a power supply voltage for supply to an external terminal.

Soeda and applicant's prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Soeda further comprising the interface as instantly claimed. The motivation for doing so, as is taught by applicant's admitted prior art, is that such a regulator circuit will lower a voltage level to prevent damage to logic or other internal circuitry while the level shifter will increase the output of the internal circuitry to produce a viable output. Therefore, it would have been obvious to combine Soeda and Applicant's prior art to obtain the invention of claims 9, 13, 29, 30, 40 and 41.

Allowable Subject Matter

6. Claims 14, 27, 31 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Regarding claims 14, 31 and 42, the prior art does not teach or suggest a device wherein a transistor of the level shifter and a device directly receiving the lower potential level signal is part of the interface circuit and is the transistor having the thinnest gate insulation film, as instantly claimed and in combination with the additionally cited elements. Regarding claim 27, the prior art does not teach or suggest a device comprising an interface circuit wherein a transistor of the interface circuit is other than one with the thinnest gate insulation film and that the interface circuit is an input buffer, as instantly claimed and in combination with the additionally cited elements.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GCE
August 19, 2004

James C. Dwyer
Director TC 2800